LASSENA: A 6.7 Megapixel, 3-sides Buttable Wafer-Scale CMOS Sensor using a novel grid-addressing architecture

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I. INTRODUCTION

In this paper we present LASSENA, a wafer scale CMOS image sensor intended for use in medical X-Ray imaging. Here we provide details of the design of this device, and some initial test results. The device is shown in Figure 1.

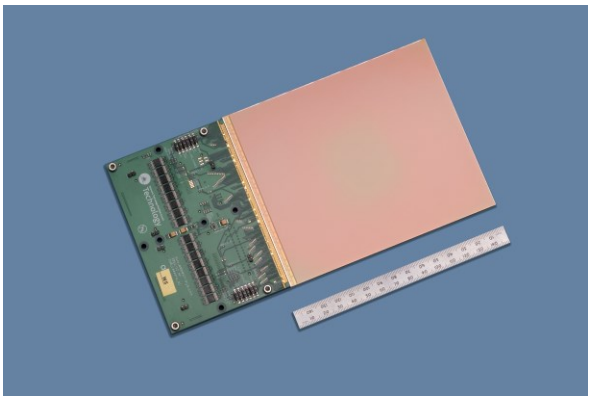

Figure 1 The LASSENA Sensor

II. LASSENA

The sensor was designed in a 180 nm, dual oxide, 5 metal, 1 poly CMOS Image Sensor process. The focal plane for LASSENA was designed to cover as much of the 200 mm wafer as possible and be 3-sides buttable. This feature allows tiling of multiple sensors in any 2xN format. A single sensor measures 120mmx145mm. The focal plane measures 120mmx140mm. This allows an imaging area of 280 mm in one direction, and any multiple of 120 mm in the other. Each sensor has a resolution of 2800 x 2400 pixels with a pitch of 50um. It is read out through 32 analogue amplifiers working at 10 Mpixel/sec. The sensor was designed using thick oxide transistors only to maximise the dynamic range.

The stitched nature of the design means it must consist of multiple identical “stitching blocks”. In order to avoid placing large blocks of logic, such as a shift register, in the array (which could lead to large artefacts), a row decoder addressing scheme was used. The decoder was placed along the only available edge – the bottom. Maintaining full addressability with this structure requires a novel addressing scheme.

The row decoders drive vertical address lines into the array. Within the array, these lines are connected to horizontal lines, to provide one address per row (Figure 2). Due to the repeating nature of the stitching blocks, one row in every block is selected by these lines.

In order to select only one of these rows, a second “block select” line is used to choose a single stitching block (Figure 3). AND gates distributed in the pixel array (figure 4), generate the select and reset signal from the row address and the block select. The gates are distributed pseudo-randomly across the array, reducing their visible effect on the image.

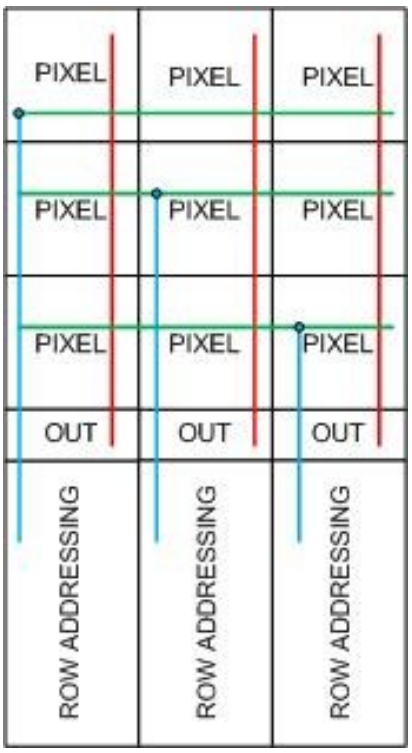

Figure 2 Row Addressing Lines

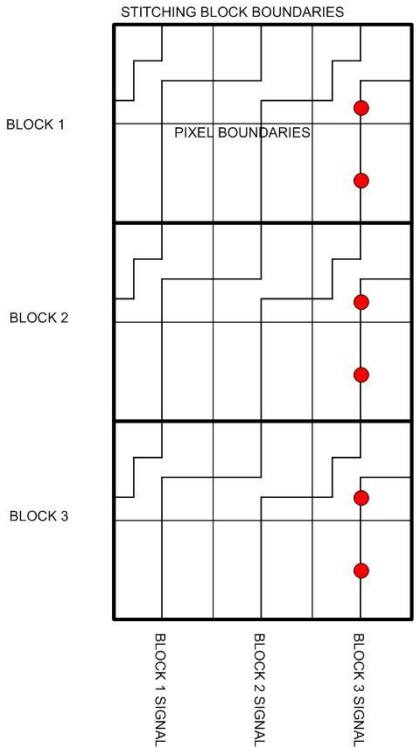

Figure 3 Block Selecting Lines

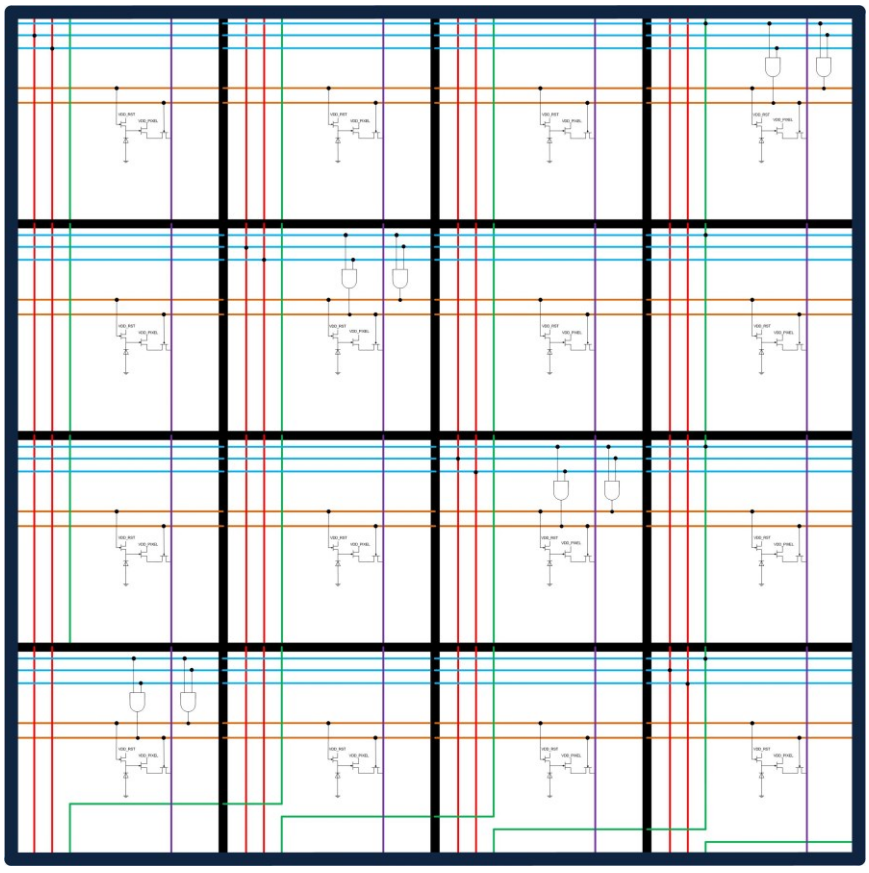

Figure 4 Full stitching block addressing (only a 4x4 pixel block is shown for clarity)

The pixel itself is based on a 3T pixel. A partially pinned photodiode [1] is used to achieve a large area diode while maintaining low noise operation. The sensor also features 2 and 4 pixel binning in both directions. The vertical binning is done in the focal plane by connecting multiple diodes according to the selected binning ratio. The horizontal binning is carried out in the periphery by connecting the sampling capacitors for two or four adjacent columns. Figure 5 shows how the switches for vertical binning are arranged in the array.

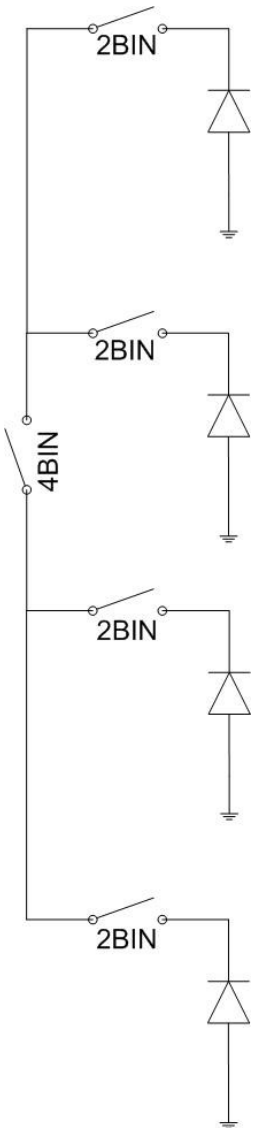

Figure 5 Arrangement of binning switches in the array of the LASSENA sensor

PMOS switches are used to connect the diodes within the array. In some pixels, extra dummy transistors are added to preserve uniformity of the array. The AND gates in the array are formed from CMOS logic in the normal way. In order to prevent the N-Wells in the pixel from collecting charge, all N-Wells are shielded using a deep P-well [2].

The row addressing is controlled by counters, which can be programmed for region-of-interest readout. Up to 6 different regions of interest can be programmed. The sensor also supports non-destructive readout as well as well as multiple reads for high-dynamic range (HDR) operation. HDR readout is performed by making use of 4 on-board row address counters. This allows 4 row address pointers to be generated. One is used to select and then immediately reset a row, giving an integration time equivalent to the frame time. The other three pointers can then be used to read out at integration times less than a full frame, giving an HDR image. This can be carried out in combination with any of the other modes of the sensor.

The sensor was designed to be radiation tolerant. For this reason, enclosed layout transistors were used throughout the design [3].

For such a large device, yield is a particular concern. To improve the yield, special care was taken in the design. For example, whenever possible minimum rules were avoided for transistor sizing, metal spacing and metal width. Single contacts and vias were also avoided. Furthermore, due to the stitched nature of the design, much important peripheral circuitry is repeated a few times across the bottom of the sensor. This includes the column and row counters. The presence of this extra circuitry was used to build redundancy into the sensor. All counters drive a common bus, but have tri-state outputs, meaning any one counter which is found to be faulty can be disconnected. In practice, all counters have functioned well, and this functionality has not been used.

III. FIRST TEST RESULTS

First results from the LASSENA sensor are described here. As mentioned in the previous sections, the sensor has several operating modes, i.e. single pixel mode, x2 binning mode, x4 binning mode, non-destructive readout for increased dynamic range and digital CDS. In this paper, we present results from the characterisation of the device in “Single Pixel Mode” in which all binning switches are open and the sensor is operated in the classic 3T mode with a single integration time.

The sensor was characterised using the PTC method [4] and a summary is shown in Table 1.

Parameter	Unit	Value
Effective Pixel pitch (X)	um	50
Effective Pixel pitch (Y)	um	50
Effective No. of pixels	Millions	6.72
Effective pixel format (X)	pixels	2,400
Effective pixel format (Y)	pixels	2,786
Frame rate	fps	34
Noise	e- rms	70.0
Conversion Gain	uV/e-	9.8
Linear Full Well Capacity	e-	112,000
Maximum Full Well Capacity	e-	144,000
Dynamic Range (linear)	dB	64.1
Dynamic Range (linear)	bit	10.6
Dynamic Range (maximum)	dB	66.3
Dynamic Range (maximum)	bit	11.0
Wavelength	nm	540
Quantum Efficiency	%	50.1

Table 1 "Single Pixel Mode" test results from the LASSENA sensor

IV. CONCLUSIONS

This work demonstrates a wafer-scale CMOS image sensor which features:

- 50 um pixels for high-resolution
- 70 e- rms noise for high sensitivity
- Video rate for high speed
- Radiation hardness

Pixels can also be binned on the sensor by 2 or 4, trading-off resolution for increased frame rate and full well. Region-of-interest readout and high-dynamic range mode with multiple readouts can also be user programmed in the sensor.

V. REFERENCES

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[4] "Comparison of Methods for Estimating the Conversion Gain of CMOS Active Pixel Sensors", S.E. Bohndiek *et al.*, *Sensors*, vol. 8, no. 10, pp. 1734 -1744, Oct. 2008